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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/667,113	09/18/2003	Gabriele Barlocchi	854063.552D1	2816

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EXAMINER	
ERDEM, FAZLI	

ART UNIT	PAPER NUMBER
2826	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/667,113	BARLOCCHI ET AL.	
	Examiner	Art Unit	
	FAZLI ERDEM	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 May 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-13,19,21 and 28-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-13,19,21 and 28-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/545,260.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1 The Finality of the action mailed on 2/5/2009 is hereby withdrawn. As Applicant pointed out in the 3/25/09 interview, the action filed 2/5/2009 failed to address claim 21, so the Final Action mailed 2/5/2009 cannot be considered complete. Further, the Non-Final Action mailed 8/1/2008 failed to address claim 21 and likewise cannot be considered complete. This Action must be considered as a replacement for the defective Non-Final Action mailed 8/1/2008.

2. The Amendment filed on 05/04/2009 has been entered.

Response to Arguments

Regarding the 35 USC 102 rejection of independent claims 28 and 32, it is argued, at page 7, paragraph 4 of the remarks filed on 10/31/2008, that "Mirza et al. is incompatible with the formation of a layer of material inhibiting epitaxial growth to cover the walls and a closed bottom of the cavity as recited in claim 28." However, in Mirza et al., the material covering the walls of the cavity is of the same oxide type material that is specified in the current application. Therefore, the oxide material of Mirza et al. should be presumed capable of inhibiting growth of epitaxial layer.

Regarding 35 USC 102 rejection on independent claims 28 and 32, it is argued, at page 6, paragraph 2 of the remarks filed on 05/04/2009, that "in contrast, Mirza et al. describe a cavity 13 that is formed in a silicon substrate 11 is covered with a diaphragm formed by a second silicon substrate 17 that is "bonded" over the top surface 12 of the first substrate". However, independent claims 28 and 32, as they currently stand, require "membrane formed of epitaxial [growth of] semiconductor material". As

explained in the following action, the limitation related to "growth" is considered a product by process limitation by examiner. Therefore, "an epitaxial layer of semiconductor material" of layer 14 Mirza et al. anticipates independent claims 28 and 32.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 28, 29, 32, and 33 are rejected under 35 U.S.C. 102(b) as being anticipated by Mirza et al. (5,883,420).

Regarding Claim 28, in Figs. 1-3, Mirza et al. disclose a wafer of monolithic monocrystalline semiconductor material 11, comprising a plurality of buried cavities 13/14, each cavity completely surrounded by said monolithic monocrystalline material 11, including membrane of epitaxial material, 14, and each cavity having walls and a closed bottom19 covered with a single coating formed of a layer of material inhibiting epitaxial growth, the plurality of buried cavities positioned adjacent to each other and separated from each other by dividers, 19.

Applicant has amended claim 28 to require the claimed membrane (which is formed from a semiconductor material) to be the product of a step of "epitaxial" growth. This requires the semiconductor membrane to be the product of a particular process

(epitaxy). However, in a device claim such as claim 28, it is the end product (the "membrane [formed] from a semiconductor material"), rather than any particular process for forming that product, that controls.

Regarding Claim 29, layer 19 is oxide.

Regarding Claim 32, in Figs. 1-3, Mirza et al. disclose a monolithic wafer of monocrystalline semiconductor material 11, comprising a plurality of buried trenches and cavity pairs each 13/14, including membrane of epitaxial material 14, each trench filled with monocrystalline material, each cavity completely surrounded by said monocrystalline material and having walls and a closed bottom19 that are covered with a single coating that is formed of a layer of material inhibiting epitaxial growth, the plurality of buried cavities positioned at different heights within the wafer of monocrystalline semiconductor material as disclosed in column 2.

Applicant has amended claim 32 to require the monocrystalline material filling each trench to be the product of a step of "epitaxial" growth. This requires the monocrystalline material forming each trench to be the product of a particular process (epitaxy). However, in a device claim such as claim 32, it is the end product (the monocrystalline material filling each trench), rather than any particular process for forming that product, that controls.

Regarding Claim 33, layer 19 is oxide.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 8-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sidner et al. (4,945,769) in view of Mirza et al. (5,883,420).

Regarding Claim 8, Figs. 2E and 2G of Sidner et al. disclose a structure formed in a substrate of monolithic semiconductor material 20, the structure comprising: at least one trench 26 formed in the substrate, the at least one trench having an open top and an open bottom, a cavity having walls formed below each at least one trench and a cavity 32 having walls and a closed bottom formed below each of at least one trench and having an open top in communication with the open bottom of the at least one trench, an epitaxial layer 14 formed in communication with the open bottom of the at least one trench, and a coating on the walls and closed bottom of the cavity with material inhibiting epitaxial growth; and an epitaxial layer 14 of semiconductor material on the substrate 20 to cover the open top of the trench and epitaxial portion formed in the at least one trench to fill the at least one trench and to encase the cavity in the substrate.

Applicant has amended claim 8 to require the epitaxial layer to be the product of a step of "horizontally and vertically" growth. This requires the epitaxial layer to be the product of a particular process. However, in a device claim such as claim 8, it is the end product (the "epitaxial layer of semiconductor material [formed] on the substrate to cover the open top of the at least one trench and formed in the at least one trench to fill

the at least one trench and to encase the cavity in the substrate"), rather than any particular process for forming that product, that controls.

Sidner et al. fail to disclose the required coating on the walls of the cavity. However, Mirza et al. disclose a semiconductor device where in Figs. 1-3; cavity 13/14 has coating 19 on the walls.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required coating on the walls of cavity in Sidner et al. as taught by Mirza et al. in order to have a semiconductor device with better insulation and reliability.

Regarding Claim 9, Figs. 1-3 of Mirza et al. disclose plurality of cavities 13/14.

Regarding Claim 10, Mirza et al. disclose the formation of cavities at different levels as disclosed in column 2

Regarding Claim 11-13, Mirza et al. disclose different cross-sectional configurations in column 2.

4. Claims 30, 31, 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mirza et al. (5,883,420) in view of Beyer et al. (4,528,047)

Regarding Claims 30, 31, 34 and 35, in Figs. 1-3, Mirza et al. discloses a monolithic/monocrystalline wafer of semiconductor material 11, comprising: a plurality of buried cavities 13/14 formed in and completely surrounded by the monolithic semiconductor material 11, each cavity of the plurality of buried cavities having only one coating 19 on at least one wall thereof consisting of a layer of oxide material inhibiting epitaxial growth. Mirza et al. fail to disclose the cavity/trench coat/liner structures to be

TEOS or nitride. However, Beyer et al. disclose a method for forming a void-free isolation structure utilizing etch and refill techniques where in Figs. 3 and 4, nitride coat/liner 30 and TEOS coat/liner 31 are disclosed.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required nitride/TEOS liner/coat in Mirza et al. as taught by Beyer et al. in order to have a semiconductor structure with better isolation.

5. Claims 19 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mirza et al. (5,883,420) in view of Sidner et al. (4,945,769)

Regarding Claims 19, 21 and 31, in Figs. 1-3, Mirza et al. disclose a structure formed in a substrate of monolithic semiconductor material 11, the structure comprising: a cavity 13/14 formed in and surrounded by the monolithic semiconductor material, the monolithic semiconductor material 11 comprising a membrane formed of epitaxial structure 17 formed on the semiconductor material 11. Mirza et al. fail to disclose the membrane have the required distance. However, Sidner et al. disclose a semiconductor device where in Fig. 1, semiconductor substrate 12 having membrane portion 14 formed of epitaxial monolithic semiconductor material monolithically integrated and part of the semiconductor substrate 12 having a thickness of between 1-10 microns. (Examiner considers newly added limitation "epitaxial growth of monolithic semiconductor material" as product by process limitation. In device claims it is the end product (i.e. epitaxial material), rather than how the epitaxial material is made i.e. "epitaxial growth of monolithic semiconductor material")

With particular regard to Claim 21, in Fig. 1 of Mirza et al. disclose etched trench passing through layers 17/19 and reaching near cavity 13/14. Furthermore, in Fig 2F of Sidner et al. trench 28 passes through layers 24 and 24 and reaches cavity 32.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required membrane portion in Mirza et al. as taught by Sidner et al. in order to have a semiconductor sensor structure with ease of manufacture and reduced geometry.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to FAZLI ERDEM whose telephone number is (571)272-1914. The examiner can normally be reached on M - F 8:00 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

FE
June 10, 2009

/Thomas L Dickey/
Primary Examiner, Art Unit 2826